What is claimed is:

1. A unit cell included in a non-volatile dynamic random access memory (NVDRAM), comprising:

a control gate layer coupled to a word line;

a capacitor for storing data;

a floating transistor for transmitting stored data in the capacitor to a bit line, gate of the floating transistor being a single layer and serving as a temporary data storage; and

a first insulating layer between the control gate layer and the gate of the floating transistor,

wherein a voltage supplied to body of the floating transistor is controllable.

2. A unit cell included in a non-volatile dynamic random access memory (NVDRAM), comprising:

a control gate layer made of a metal and coupled to a word line;

a capacitor for storing data; and

a floating transistor for transmitting stored data in the capacitor to a bit line, gate of the floating transistor being a single nitride layer and serving as a temporary data storage,

wherein a voltage supplied to body of the floating transistor is controllable.

3. A non-volatile dynamic random access memory (NVDRAM) device for controlling a unit cell, comprising:

an internal voltage generator for receiving an external voltage and generating a plurality of internal voltages having each different level;

a switching means for supplying one of the plurality of internal voltages to a word line, a bit line and a capacitor plate line; and

a mode controller for controlling the switching means.

4. The circuit as recited in claim 3, wherein the switching means includes:

a word line voltage switch block for supplying one of the plurality of internal voltages to the word line;

a bit line precharge voltage switch block for supplying one of the plurality of internal voltages to the bit line; and

a plate line voltage switch block for supplying one of the plurality of internal voltages to the capacitor plate line.

5. The circuit as recited in claim 3, wherein the plurality of internal voltages is in range of about -5V to about +5V.

6. The circuit as recited in claim 3, wherein the mode controller controls the switching means for operating in a normalization mode that the unit cell is operated as a unit cell of a dynamic random access memory by adjusting a

threshold voltage of a floating gate in the unit cell.

7. The circuit as recited in claim 6, wherein the mode controller controls the switching means for operating in a recall mode that data stored in the floating gate in the unit cell is restored in a capacitor in the same unit cell when the external voltage is supplied.

8. The circuit as recited in claim 7, wherein the mode controller controls the switching means for operating in a program mode that data stored in the capacitor in the unit cell is loaded in the floating gate in the same unit cell before the external voltage is exhausted after the external voltage is isolated.

9. The circuit as recited in claim 8, further including:

an external voltage monitoring means for detecting an isolation of the external voltage directly; and

a storage battery for operating the unit cell during a predetermined time when the external voltage is isolated.

10. The circuit as recited in claim 3, further comprising:

a backup memory cell block for backing up data stored in each unit cells.

11. The circuit as recited in claim 10, wherein a backup

data size is based on a size of the backup memory cell block.

12. The circuit as recited in claim 11, wherein the size of the backup memory cell block is same to that of each memory cell blocks.

13. The circuit as recited in claim 3, wherein the unit cell has a floating gate for storing data when the external voltage is isolated.

14. The circuit as recited in claim 3, wherein the unit cell has a silicon-oxide-nitride-oxide-silicon (SONOS) structure.

15. The circuit as recited in claim 3, wherein the unit cell has a metal-nitride-oxide-silicon (MNOS) structure.

16. A method for operating a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising the steps of:

(A) charging the capacitors of all memory cell with a logic HIGH datum; and

(B) discharging the capacitor in the memory cell having the transistor, its floating gate storing a logic high datum.

17. The method as recited in claim 16, further

comprising the step of (C) refreshing the plurality of capacitors.

18. The method as recited in claim 17, wherein the plurality of the memory cells are arranged in a matrix by using a number of word lines and bit lines and the step (C) is carried out in a row-by-row basis.

19. The method as recited in claim 16, wherein the step (A) includes the steps of:

(A-1) supplying one word line connected to a multiplicity of the memory cells with a first threshold voltage in order to turn on the transistors in all of the memory cells;

(A-2) writing the logic HIGH datum in the capacitors of the memory cells coupled to the word line; and

(A-3) repeating the steps (A-1-a) and (A-1-b) until all of the capacitors in the plurality of the memory cells are charged with the logic HIGH datum.

20. A method for operating a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising the steps of:

(A) supplying a word line with a voltage defined by the following equation:

$$V_{wl} = V_{blp} + (V_{th-H} + V_{th-L})/2$$

where V_{blp} is a bit line precharge voltage, V_{th-H} is a first target threshold voltage, and V_{th-L} is a second target threshold voltage; and

(B) writing logic HIGH or LOW data in the capacitor in response to whether the threshold voltage is the V_{th-H} or the V_{th-L}.

21. The method as recited in claim 20, further comprising:

(C) refreshing the plurality of memory cells by supplying each word line with a voltage which is higher than the logic HIGH datum

22. The method recited in claim 20, wherein the step (A) includes the step of (A-1) supplying other word lines with a predetermined negative voltage except for the word line supplied with the 'V_{wl}'.

23. A method for operating a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising the steps of:

(A) supplying all gates of the transistors in all of the memory cells with a first predetermined voltage in order for fulfilling electrons in the floating gate;

(B) charging all of the capacitors in all of the memory cells;

(C) decreasing the threshold voltage of the transistors to the first threshold voltage.

24. The method as recited in claim 23, further comprising:

(E) backing up the captured data in the capacitor before the step (A); and

(F) restoring the backup data in the capacitor after the step (C).

25. The method as recited in claim 23, wherein the step (B) includes the steps of:

(B-1) supplying one side of the capacitor with about 0 V; and

(B-2) supplying the bit line with the logic HIGH datum.

26. The method as recited in claim 23, wherein the step (C) includes the steps of:

(C-1) removing electrons in the floating gate of the memory cells;

(C-2) discharging the capacitor by supplying gate of the transistor in the memory cells with the first threshold voltage; and

(C-3) repeating the steps (C-1) to (C-2) until all of the capacitors is discharged.

27. The method as recited in claim 26, wherein the step

(C-1) includes the steps of:

(C-1-a) supplying a gate of the transistor in all of the memory cells with a negative voltage;

(C-1-b) supplying a plate of the capacitor in the memory cells with voltage level of a logic HIGH datum; and

(C-1-c) moving electrons in the floating gate to the capacitor storing the logic HIGH datum.

28. The method as recited in claim 26, wherein the step (C-2) includes the steps of:

(C-2-a) supplying the gate of the transistor with a second threshold voltage; and

(C-2-b) discharging the capacitor in some of the memory cells having the transistor turned on by the second threshold voltage.

29. The method as recited in claim 26, wherein the step (C) includes the step of (C-4) refreshing all of the memory cells.

30. The method as recited in claim 29, wherein the plurality of the memory cells are arranged in a matrix by using a number of word lines and bit lines and the step (C) is carried out in a row-by-row basis.

31. The method as recited in claim 30, wherein the capacitor is a coupling capacitor.

32. A method for operating a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising the steps of:

(A) removing electrons in the floating gate of the memory cell storing a logic HIGH datum;

(B) discharging the capacitor by supplying gate of the transistor in all of the memory cells with a second threshold voltage; and

(C) repeating the steps (A) to (B) until all of the capacitors is discharged.

33. The method as recited in claim 32, wherein the step (A) includes the steps of:

(A-1) supplying a gate of the transistor in all of the memory cells with a negative voltage;

(A-2) supplying a plate of the capacitor in the memory cells with voltage level of a logic HIGH datum; and

(A-3) selectively moving electrons in the floating gate to the capacitor storing the logic HIGH datum.

34. The method as recited in claim 33, wherein the step (B) includes the steps of:

(B-1) supplying the gate of the transistor with a second threshold voltage; and

(B-2) discharging the capacitor in some of the memory cells having the transistor turned on by the second threshold

voltage.

35. The method as recited in claim 34, wherein the step (B) includes the steps of (B-c) refreshing the memory cell.

36. The method as recited in claim 35, wherein the step (B) is carried out row-by-row.

37. The method as recited in claim 36, wherein the capacitor is a coupling capacitor.

38. The circuit as recited in claim 3, wherein the unit cell has a silicon-oxide-nitride-oxide-silicon (SONOS) structure.

39. The circuit as recited in claim 3, wherein the unit cell has a metal-nitride-oxide-silicon (MNOS) structure.